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Conductance fluctuations from the local alteration of a hopping path

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Abstract. Conductance fluctuations are observed in a narrow Si MOSFET below threshold at low temperatures as the laterally confining potential well is shifted perpendicular to the current direction by application of a transverse voltage ΔV_p. A calculation is presented of the spatial shift as a function of ΔV_p which suggests that the physical origin is a gradual modification of the percolation path in both the energy and spatial coordinates.

1. Introduction

Fluctuations near threshold in the conductance g as a function of the gate voltage V_g have been observed in FET devices for many years (see, e.g., Kaplan 1988, Kwasnick *et al* 1984, Pepper and Uren 1982, Webb *et al* 1985). Theoretical work has related the observed structure to the sample-specific random arrangement of localised states. Lee (1984) showed that in hopping conduction a non-monotonic dependence of the sample resistance on the Fermi energy E_F is possible. Certain experimentally observed features of the conductance fluctuations can be explained in terms of one or two 'critical hops' limiting the current. In short samples at very low temperatures conduction can proceed by direct tunnelling in and from a single localised state near the centre of the resistance-dominating region, the model of resonant tunnelling (Azbel and DiVincenzo 1984, Stone and Lee 1985).

Si MOSFETs have been designed and studied by several groups in which p^+ implants on either side of a typically 1 μm wide gate create a narrow confining potential well perpendicular to the current direction as first suggested by Pepper (Dean and Pepper 1982). The fluctuations in the conductance versus gate voltage have been studied in considerable detail with this type of device (Fowler *et al* 1982). In the present work a new type of experiment is performed in order to gain more insight into this widely observed phenomenon. The conductance is measured as the minimum of the potential well is continuously shifted across the available area under the gate. This is achieved by sweeping the voltage difference $\Delta V_p = V_{p1} - V_{p2}$ between the two p^+ implants. The gate voltage V_g and the average confining voltage $V_p = (V_{p1} + V_{p2})/2$, both measured with respect to the source potential, are kept constant. On top of a smooth background, conductance fluctuations of typically 50% relative magnitude are observed at $T = 4.2$ K. Certain simplifying assumptions allow the corresponding electrostatic problem to be solved analytically in a generalisation of Shik's calculation (Shik 1985) of the symmetric case $V_{p1} = V_{p2} = V_p$. The position of the potential minimum x_{min} is calculated allowing ΔV_p to

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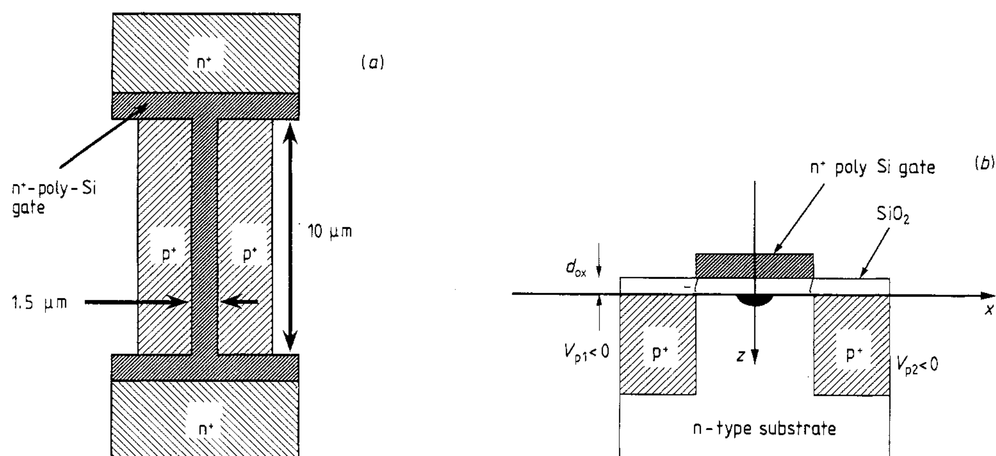

Figure 1. Top view and cross section of the devices used in the experiments. In (*b*) the shaded area around the origin indicates the position of the channel for the symmetric case where ($\Delta V_p = 0$) above threshold.

be related to a spatial coordinate. The shape of the potential in the vicinity of the potential minimum allows the physical origin of the observed fluctuations to be determined.

2. Experiments

The devices used in the experiments are silicon accumulation layer MOSFETs with a lithographically defined channel of size 1.5 μm $\times$ 10 μm and p^+ implants on either side of the gate as shown in figure 1(*a*). They have been designed by D M Pooke (Pooke *et al* 1988). The self-aligned p^+ implants are expected to extend less than 0.1 μm underneath the gate (Gundlach 1989). The potential well perpendicular to the current direction is determined by the (positive) gate voltage and the (negative) voltages V_{p1}, V_{p2}, applied to the two p^+ implants. The source and drain consist of wide regions of the gate and n^+ implants, which in turn form Ohmic contacts with the Al metallisation. The narrow part of the gate turns on at higher gate voltages than the wide one and therefore determines the resistance of the device even at $V_p = 0$ V. The substrate is a 50 Ω cm n-type Si wafer—corresponding to 8.4×10^{13} cm^{-3} phosphorus atoms and a typical donor separation of 230 nm—and transistors with gate oxide thicknesses d_{ox} of 60 and 400 nm were used. It is important to note that although the device is an accumulation layer MOSFET, the substrate is depleted between the p^+ implants; that is, a depletion charge N_{depl} is present. A cross section through the channel is shown in figure 1(*b*), where the coordinates used in the calculation are also defined.

In the experiments, AC source–drain voltages in the range 10 to 100 μV and frequencies between 80 and 125 Hz were applied and the current was measured using standard lock-in techniques. DC techniques were found to give the same results but were not used for the measurements here as the required source–drain voltages were unacceptably high. Either ΔV_p was swept keeping V_g constant or vice versa. The high resistances measured required the use of separately screened leads to source and drain contacts in order to reduce stray capacitances to below 10^{-14} F. The data were taken with the lock-in amplifier set to a short integration time and was recorded by a computerised acquisition system, after which it could be digitally averaged and filtered. The filter roll-off was chosen such that data taken with increasing and decreasing voltages respectively

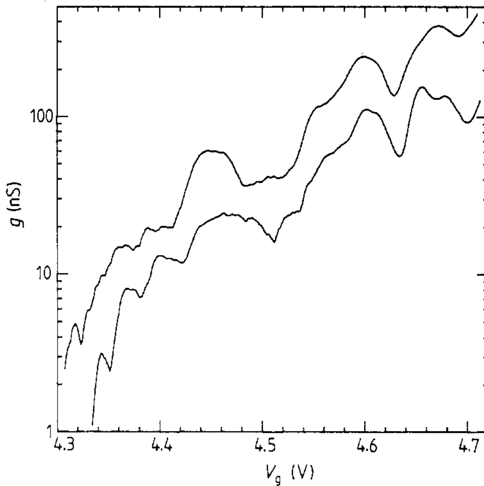

Figure 2. Conductance as a function of gate voltage at $T = 4.2$ K (top curve) and 1.4 K (bottom curve), with $V_p = -9.3$ V, $\Delta V_p = 0$ V, for the device with $d_{ox} = 60$ nm.

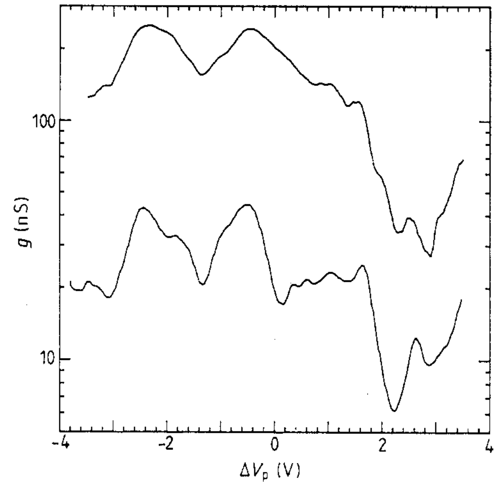

Figure 3. Conductance as a function of transverse voltage ΔV_p at $T = 4.2$ K (top curve) and 1.4 K (bottom curve), with $V_g = 4.66$ V, $V_p = -9.3$ V, for the device with $d_{ox} = 60$ nm.

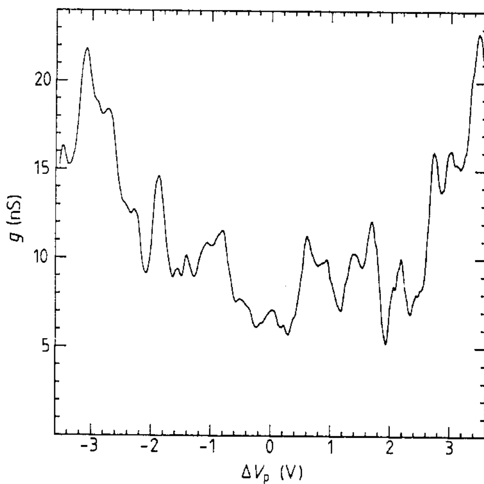

Figure 4. Conductance as a function of transverse voltage ΔV_p at $T = 4.2$ K, with $V_g = 18.7$ V, $V_p = -9.3$ V, for the device with $d_{ox} = 400$nm.

were indistinguishable. For sweeps with increasing and decreasing ΔV_p a slight hysteresis was observed, more significant at higher gate voltages and lower temperatures, presumably due to spatial redistribution of the occupancy of band tail states and Si–SiO_2 interface states in the varying transverse field. It was found that it is advantageous to keep ΔV_p constant and sweep V_g because in the course of several days the threshold voltage V_T was found to wander around by up to ± 20 mV while the structure in the conductance as a function of $V_g - V_T$ had a good long-term reproducibility.

In figure 2 typical data $g(V_g)$ at temperatures 4.2 and 1.4 K are shown of a transistor with $d_{ox} = 60$ nm. Typical g versus ΔV_p curves are shown in figures 3 and 4 for devices with oxide thicknesses 60 and 400 nm respectively. The overall increase of the conductance with increasing magnitude of ΔV_p is always observed and more significant at lower gate voltages. The features have different typical scale for the two oxide thicknesses. Figure 5 shows the development of the structure as both ΔV_p and V_g are varied

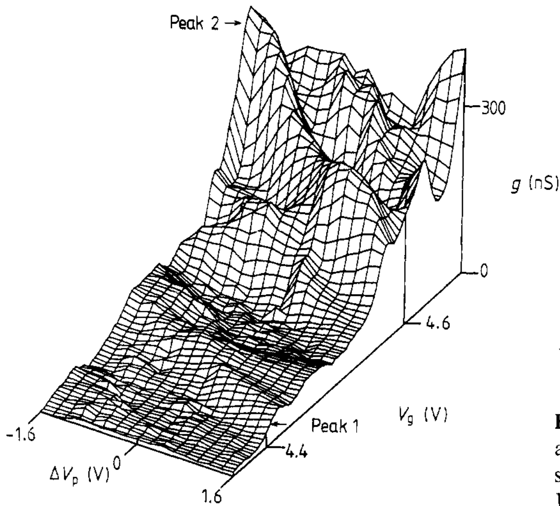

Figure 5. Conductance as a function of both gate and transverse voltage at $T = 4.2$ K. The grid has spacings of 0.2 V on the ΔV_p axis and 4 mV on the V_g axis. $V_p = -9.3$ V, $d_{ox} = 60$ nm.

for a smaller range of ΔV_p for which the average conductance is fairly constant. No systematic investigation of the detailed temperature dependence has been undertaken so far but preliminary results indicate a saturation of the conductance after an initial decrease as the temperature is lowered from 4.2 to 1.2 K. At these temperatures no difference in the temperature dependences of the amplitudes of the peaks and valleys in $g(V_g)$ is seen. The range of stronger temperature dependence is too small to distinguish between possible values of $n = 1, \frac{1}{2}$ and $\frac{1}{3}$ in $g \propto T^{-n}$ law.

3. Calculations

Under certain simplifying assumptions we obtain an analytical expression for the potential at the Si–SiO_2 interface in a generalisation of Shik's calculation (Shik 1985). The potential in the depleted region between the p^+ implants obeys Poisson's equation

$$\partial^2\varphi/\partial x^2 + \partial^2\varphi/\partial z^2 = -N_{depl}/\varepsilon_0\varepsilon^{Si} \tag{1}$$

whereas in the oxide it is given by Laplace's equation

$$\partial^2\varphi^{ox}/\partial x^2 + \partial^2\varphi^{ox}/\partial z^2 = 0. \tag{2}$$

In general (1) and (2) have to be solved simultaneously for the boundary conditions

$$\varphi(x = -l) = V_{p1} \qquad \varphi(x = l) = V_{p2} \qquad \varphi(z \to \infty) = 0 \tag{3}$$

where the p^+–n built-in potential of the order of -1 V is included in V_{p1} and V_{p2}. Following Shik's argument, the situation $d_{ox} \ll 2l$ allows the solution of Laplace's equation to be approximated by

$$\varphi^{ox}(x, z) \simeq (1 + z/d_{ox})\varphi^{ox}(x, 0) - (z/d_{ox})V_g \tag{4}$$

and also allows fringing fields at the margins of the gate to be neglected. In the limit of no accumulation or trapped oxide charge being present—the situation well below threshold—the dielectric boundary condition at the Si–SiO_2 interface reduces to

$$\varepsilon^{ox}(\partial\varphi^{ox}/\partial z)|_{z=0} = \varepsilon^{Si}(\partial\varphi/\partial z)|_{z=0} \tag{5}$$

Equations (4) and (5) may be written in the form

$$(\partial\varphi/\partial z)|_{z=0} = (\varepsilon^{\rm ox}/\varepsilon^{\rm Si} d_{\rm ox})(\varphi(x,0) - V_{\rm g}). \tag{6}$$

The solution of equation (1) obeying the boundary conditions equations (3) and (6) is

$$\begin{aligned}\varphi(x,z) = {} & \frac{N_{\rm depl}}{2\varepsilon_0\varepsilon^{\rm Si}}(l^2 - x^2) + \frac{l-x}{2l}V_{\rm p1} + \frac{l+x}{2l}V_{\rm p2} \\ & + \sum_{k=0}^{\infty} A_k \cos\left(\frac{\pi x}{2l}(2k+1)\right)\exp\left(-\frac{\pi}{2l}(2k+1)z\right) \\ & + \sum_{k=1}^{\infty} B_k \sin\left(\frac{\pi x}{l}k\right)\exp\left(-\frac{\pi k}{l}z\right)\end{aligned} \tag{7}$$

with

$$\begin{aligned} A_k &= \frac{(-1)^k}{1 + [\pi/(2lL)](2k+1)}\left(\frac{4(V_{\rm g} - V_{\rm p})}{\pi(2k+1)} - \frac{16kl^2}{\pi^3(2k+1)^3}\right) \\ B_k &= \frac{(-1)^{k+1}(V_{\rm p1} - V_{\rm p2})}{\pi(1 + \pi k/lL)k}. \end{aligned} \tag{8}$$

The approximations used apply strictly only to the regime well below threshold where no accumulation charge is present and where the Fermi energy is below the tail of the conduction band. A significant amount of mobile charge would greatly complicate this analysis because $E_{\rm c} - E_{\rm F}$ is not constant across the channel, so the occupancy of these states would not be constant either. But as hysteresis effects were small when the channel was shifted sideways, we can say that at least states within a certain range of time constants play a minor role. Only a weak dependence of the results of calculations based on equations (7) and (8) on the parameters $N_{\rm depl}$, l and $d_{\rm ox}$ was found, in the sense that their uncertainty in the present experimental situation can be neglected.

For $d_{\rm ox} = 60$ nm, $l = 0.7\ \mu$m and $N_{\rm depl} = 8 \times 10^{13}$ A s cm^{-3}, corresponding to phosphorus-doped Si with a resistivity $\rho_{300\rm K} = 50\ \Omega$ cm, figure 6 shows the potential across the channel for $\Delta V_{\rm p} = 0$ V and $\Delta V_{\rm p} = 4$ V. In an energy range of many $k_{\rm B}T$ the potential minimum is parabolic with a curvature as given in table 1. It is sharper for the thicker gate oxide but it should be noted that in this case $d_{\rm ox} \ll 2l$ is not strictly valid. In figure 7 the minimum is plotted for various $\Delta V_{\rm p}$. The inset displays the dependence on $\Delta V_{\rm p}$ of the position of the minimum $x_{\rm min}$. This dependence was found to become non-linear only at appreciably higher $\Delta V_{\rm p}$ than was applied in the experiments, when $x_{\rm min}$ approaches $\pm l$. From the inset of figure 7 one finds that the slope is $dx_{\rm min}/d(\Delta V_{\rm p}) =$ 21 nm V^{-1} for $d_{\rm ox} = 60$ nm whereas it is $dx_{\rm min}/d(\Delta V_{\rm p}) = 24$ nm V^{-1} for $d_{\rm ox} = 400$ nm. The parameters chosen for the calculation of these graphs are such that the gate voltage differs by less than 0.1 V from the calculated threshold voltage, defined by the condition $E_{\rm c} - E_{\rm F} = 0$ at $x = x_{\rm min}$. Within this range the position and curvature of the minimum is virtually unique, so some constant offset of say 100 meV to the potential does not matter. The threshold voltages found experimentally are somewhat larger, presumably due to occupied states in the oxide and the band tail of localised states. Because additional charges are neglected in the calculation the results have to be interpreted as approximations that lose validity as the experimental threshold is approached.

For $d_{\rm ox} = 60$ nm, $E_{\rm c} - E_{\rm F}$ at the potential minimum varies at a rate of 0.8 eV V^{-1} with gate voltage. This is the maximum rate to be expected in the experiments whereas the minimum rate is given by the MOS capacitor relation as 2.3 meV V^{-1}, neglecting the minor contribution from the variation of the energy difference between the lowest sub-band and $E_{\rm c}$ due to the dependence on the accumulation charge of the shape of the

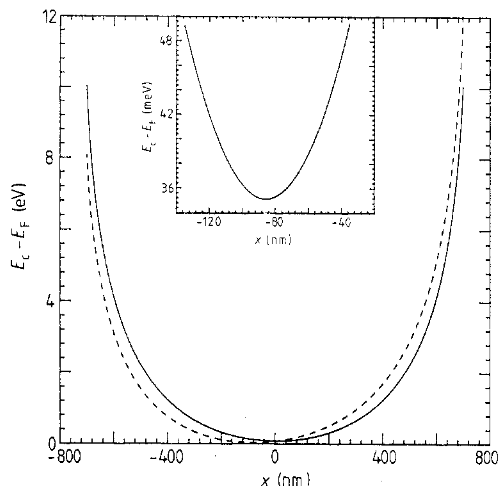

Figure 6. The calculated potential below the narrow part of the gate at the Si–SiO_2 interface as a function of the distance from the channel centre for $V_g = 3.0$ V, $V_p = -10.3$ V, $\Delta V_p = 0$ V (full curve, $\Delta V_p = 4$ V (broken curve) and $d_{ox} = 60$ nm. The inset shows the vicinity of the potential minimum for $\Delta V_p = 4$ V where it is identical to a fitted parabola on this scale.

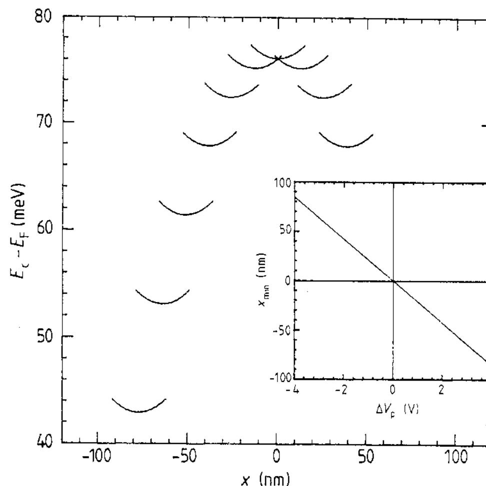

Figure 7. The calculated shape of the potential minimum for $V_g = 3.0$ V, $V_p = -10.3$ V, $d_{ox} = 60$ nm and $\Delta V_p = +3.6$ V, $+3.2$ V, . . ., -1.8 V. The inset shows the position of the minimum for the same parameters with ΔV_p between -4.0 V and $+4.0$ V.

Table 1. Curvature of the parabolic potential minimum (in meV nm^{-2}).

	$\Delta V_p = 0.0$ V	$\Delta V_p = 4.0$ V
$d_{ox} = 60$ nm	5.62×10^{-3}	5.69×10^{-3}
$d_{ox} = 400$ nm	1.19×10^{-2}	1.21×10^{-2}

potential well confining the electrons in the z direction. The region of the transition between these two limits is determined essentially by the DOS (density of states) in the band tail.

4. Discussion

The overall increase of the conductance with increasing $|\Delta V_p|$ as apparent in figure 4 corresponds to the shift of the potential minimum to lower energies depicted in figure 7. For ΔV_p increasing from 0 to 3.6 V this shift is 33 meV ($d_{ox} = 60$ nm) or 87 meV ($d_{ox} = 400$ nm). The experimentally observed effect is considerably smaller than what would be expected from this shift by many k_BT. This can be interpreted as evidence for the occupation of band tail states as threshold is approached. The energy of the minimum was calculated to change at a rate of 800 meV V^{-1} ($d_{ox} = 60$ nm) or 300 meV V^{-1} ($d_{ox} = 400$ nm) with gate voltage while its position remains unaffected in the region around theoretical threshold. For $d_{ox} = 400$ nm one expects from this the increase of the conductance from $\Delta V_p = 0$ to $\Delta V_p = 3.6$ V to be of the same order of magnitude as would be seen for a gate voltage increase of 0.29 V. This was found to be approximately the case. No such effect is apparent in figure 3 which shows the analogous result for a device

with $d_{ox} = 60$ nm. This is mainly due to the weaker dependence of the channel position on ΔV_p for the thinner oxide but could also indicate the presence of large-scale inhomogeneities across the channel.

We now discuss the structure observed in the conductance. The peaks cannot be simply due to the conducting channel probing regions of smaller and larger transmission coefficient caused by ever-present inhomogeneities. This can be concluded from the fact that for $d_{ox} = 60$ nm the potential minimum with a curvature of 5.7×10^{-3} meV nm^{-2} (table 1) has a width of 22 nm on an energy scale of $2k_BT|_{4.2K} = 0.72$ meV, so the peak width in $g(\Delta V_p)$ should be at least $\delta(\Delta V_p) = 22$ nm/21 nm V$^{-1} \simeq 1.0$ V. The observed structure is sharper than this (figure 3).

The model of resonant tunnelling, mentioned in the introduction, can be regarded as hopping conduction in the limit of only one localised state mediating between the source and drain Fermi seas. Although the relevance of this model to this work cannot be ruled out completely—there is the possibility of a short potential barrier limiting the current as discussed below—the phenomenon is expected to be observable only at mK temperatures and to show up in the conductance versus gate voltage as well separated sharp peaks on top of a slowly varying background. We therefore seek for an interpretation within the framework of the hopping conduction theory.

The energy of a localised state relative to the Fermi energy is the sum of its energy relative to the conduction band minimum and the energy difference $E_c - E_F$ calculated in the last section. We consider the energy difference between two subsequent localised states of a hopping path having a separation of, say, 20 nm in the direction perpendicular to the channel and some arbitrary distance along it. The question is by how much ΔV_p has to be changed in order to alter their energy difference by, say, $4k_BT|_{4.2K}$, just enough to convert a difficult hop into an easy one and back again. The minimum shown in the inset of figure 6 (device with $d_{ox} = 60$ nm) can be approximated by $E_c - E_F = A(x - B)^2 + C$ with $A = 5.69\ 10^{-3}$meV nm^{-2}, $B = 85.4$ nm and $C = 35.1$ meV. Suppose the two states are at x_1 and x_2, where $x_1 - x_2 = 20$ nm, and have energies D_1 and D_2 relative to the conduction band, where $D_1, D_2 < 0$, such that their energies E_1 and E_2 are the same with respect to the Fermi level, that is

$$A(x_1 - B)^2 + C + D_1 = A(x_2 - B)^2 + C + D_2.$$

For the distance Δx by which the potential well has to be shifted in order to separate E_1 and E_2 by ΔE we find the relation

$$\Delta x = \Delta E/2A|x_1 - x_2|.$$

A typical peak half-width would correspond to $\Delta E \geqslant 4k_BT|_{4.2k} = 1.45$ meV. For $x_1 - x_2 = 20$ nm, we obtain $\Delta x = 6.4$ nm or $\delta(\Delta V_p) = 0.3$ V. If the resistance is dominated by two states closer together in the x direction, a broader peak will appear. This estimate is consistent with the experimental result in figure 3. For $d_{ox} = 400$ nm the curvature of the potential minimum is larger, $A = 1.2 \times 10^{-2}$ meV nm^{-2} giving $\Delta x = 3.0$ nm. It is $\mathrm{d}x_{min}/\mathrm{d}(\Delta V_p) = 24$ nm V^{-1} and the typical peak width 0.13 V. In the range $\Delta V_p = \pm 3.6$ V one can expect about 20 to 30 distinguishable peaks. This compares well with figure 4.

In the description given above the structure in $g(\Delta V_p)$ is interpreted as originating from the effect of the confining potential on the characteristics of the critical hop, which dominates the sample resistance. Different peaks correspond to different pairs of states forming the 'bottleneck'. The development of the conductance in the $(V_g, \Delta V_p)$-plane (see figure 5) can be explained within this picture as follows. Firstly it should be noted

that the current will flow predominantly over a region of width w centred at the potential minimum, assuming the band tail has a strongly decreasing DOS away from the mobility edge. A typical value for $w/2$ could be the distance from the minimum to where the potential is $2k_BT$ higher. For a curvature of 5.7×10^{-3} meV nm^{-2} this gives $w = 22$ nm which is of the same order of magnitude as that at which Fowler *et al* (1982) find 1D hopping conduction in a similar transistor at lower temperatures. At a given position the rate of change of $E_c - E_F$ with ΔV_p,

$$d(E_c - E_F)/d(\Delta V_p) = [d(E_c - E_F)/dx]\, dx/d(\Delta V_p)$$

will typically be given by the potential slope at a distance of, say, 4 nm away from the minimum, which yields a value $d(E_c - E_F)/d(\Delta V_p) = 0.96$ meV V^{-1} in our example. This assumes that $E_c - E_F$ changes with ΔV_p only because of the curvature of the potential minimum. As we discussed at the beginning of this section it is reasonable to neglect the dependence of the offset to the potential minimum on ΔV_p because the experiments show that this effect is appreciably smaller than predicted by the calculation; see figure 7. On the other hand an ideal MOS capacitor with $d_{ox} = 60$ nm will follow the relation

$$d(E_c - E_F)/dV_g = R \times 2.3 \text{ meV V}^{-1}$$

if the DOS is reduced by a factor R at the position of E_F in the band tail. This allows us to estimate that a peak appearing at some gate voltage V_g should move to $V_g + \delta V_g$, where $\delta V_g = \alpha\delta(\Delta V_p)$ and $\alpha = 0.96/2.3R = 0.42/R$, as ΔV_p is changed to $\Delta V_p + \delta(\Delta V_p)$. From figure 5 we find for the peaks 1 and 2 in the lower and higher-conductance regime respectively

$\alpha = 0.017, R = 25$ (at $V_g = 4.4$ V) $\qquad \alpha = 0.02, R = 21$ (at $V_g = 4.65$ V).

Peaks appearing while the corresponding pair of states is close to the minimum will of course have a smaller α. It is obvious that depending on the states sitting on either side of the potential well α can have either sign.

According to Lee (1984) the slope of the peaks in a plot of $\ln(g)$ versus V_g is expected to be $1/k_BT$ if the gate voltage is converted to the appropriate energy scale. This allows us to determine R independently. We find $R = 11$ and $R = 5$ for the same two peaks. These values are somewhat smaller than those above, not quite consistent even considering the assumptions involved and also the fact that the peaks are not very well isolated at 4.2 K, which reduces the slopes in $g(V_g)$.

No peak should persist when the minimum is shifted by more than say 20 nm, equivalent to $\delta(\Delta V_p) = 1.0$ V. Inspecting figure 5 one does indeed find a correlation scale in ΔV_p of this order of magnitude. Concerning the structure in $g(V_g)$ we mention that for $R = 8$ it is $d(E_c - E_F)/dV_g = 18$ meV V^{-1} implying that $\delta E_F = k_BT|_{4.2\text{K}} = 0.36$ meV corresponds to $\delta V_g = 0.02$ V which is close to the resolution of figure 5; the dominant peaks are separated by more than this value.

An open question remains as to whether or not only a short portion of the 10 μm long channel dominates the sample resistance. The explanation offered for the observed effects clearly does not require a barrier longer than a few hopping lengths. In devices avalanched at high DC source–drain fields, charges injected into the oxide form a potential barrier typically 100 nm long close to the drain contact—at a positive potential relative to the source—and significantly increase the structure in $g(V_g)$ (Pepper and Uren 1982). In intermediate DC source–drain fields up to $V_{sd}/L = 10^3$ V m^{-1} we observed non-linear $g(V_{sd})$ characteristics similar to those reported by Kwasnick *et al* (1984). In

our case the curves could be fitted by the model of a short barrier exhibiting activationless hopping in series with a smaller, constant resistor. A definitive conclusion could not be reached but it should be noted that in such a situation the dependence of the conductance on, for instance, the temperature could be obscured. Also resonant tunnelling could be observable even in a nominally 10 μm long device.

5. Conclusion

In narrow-Si-accumulation-layer MOSFETs based on field-confinement technology we observe fluctuations in the conductance as a function of a transverse voltage ΔV_p added to the confining voltage $V_p < 0$. In order to trace back possible origins of this structure, we calculate the transverse potential in the approximation of no mobile charge being present. Using these results we show that a consistent description emerges if we relate the experimentally controlled transverse potential to the alignment in the energy coordinate of two localised states forming the 'critical hop' in a certain hopping path. The relative magnitude of the fluctuations implies that only a very small number of parallel hopping paths carry the current, so no statistical averaging can occur. The conducting part of the device is sufficiently narrow well below threshold, with the DOS considerably reduced below the free-electron value as we show. The strong functional dependence $g(\Delta V_p)$ explains why these transistors tend to be fairly noisy around threshold when nominally the same voltage is applied to the confining p^+ electrodes.

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